

IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

Listing of Claims

Claims 1-16 (canceled).

17. (currently amended) A signal processing circuit comprising:
an equalizer for equalizing an input signal based on partial response
characteristics having $(1 - D^2)$;

a discrete filter for converting the output from said equalizer into a an asymmetrical waveform of $(1 - D^2)$ ($c_0 + c_1D + \dots + c_nD_n$); and
a maximum-likelihood-demodulator for demodulating data output from said
discrete filter,
wherein said coefficients ($c_0, c_1 \dots c_n$) are integer numbers.

18. (currently amended) A signal processing circuit comprising:
an equalizer for equalizing an input signal based on partial response
characteristics having $(1 - D^2)$;
a discrete filter for converting the output from said equalizer into a waveform
of $(1 - D^2)$ ($c_0 + c_1D + \dots + c_nD_n$); and
a maximum-likelihood-demodulator for demodulating data output from said
discrete filter according to claim 17,
wherein the output waveform of said discrete filter is $(1 - D^2)$ ($c_0 + c_1D + c_2D^2$), the coefficients (c_0, c_1, c_2) are (3, 2, 1) respectively.

19. (currently amended) A signal processing circuit comprising:
an equalizer for equalizing an input signal based on partial response characteristics having $(1 - D^2)$;
a discrete filter for converting the output from said equalizer into a waveform of $(1 - D^2) (c_0 + c_1D + \dots + c_nD_n)$; and
a maximum-likelihood-demodulator for demodulating data output from said discrete filter according to claim 17,
wherein the output waveform of said discrete filter is $(1 - D^2) (c_0 + c_1D^2)$, and the coefficients (c_0, c_1, c_2) are $(5, 4, 2)$ respectively.

20. (currently amended) A signal processing circuit comprising:
an equalizer for equalizing an input signal based on partial response characteristics having $(1 - D^2)$;
a discrete filter for converting the output from said equalizer into a waveform of $(1 - D^2) (c_0 + c_1D + \dots + c_nD_n)$; and
a maximum-likelihood-demodulator for demodulating data output from said discrete filter according to claim 17,
wherein the output waveform of said discrete filter is $(1 - D^2) (c_0 + c_1D + c_2D^2)$, and the coefficients (c_0, c_1, c_2) are $(2, 2, 1)$ respectively.

21. (currently amended) A signal processing circuit comprising:

an equalizer for equalizing an input signal based on partial response characteristics having $(1 - D^2)$;
a discrete filter for converting the output from said equalizer into a waveform of $(1 - D^2) (c_0 + c_1D + \dots + c_nD_n)$; and
a maximum-likelihood-demodulator for demodulating data output from said discrete filter according to claim 17,
wherein the output waveform of said discrete filter is $(1 - D^2) (c_0 + c_1D^2 + c_3D_3)$, and the coefficients (c_0, c_1, c_2, c_3) are $(2, 5, 3, 2)$ respectively.

22. (currently amended) A signal processing circuit comprising:
an equalizer for equalizing an input signal based on partial response characteristics having $(1 - D^2)$;
a discrete filter for converting the output from said equalizer into a waveform of $(1 - D^2) (c_0 + c_1D + \dots + c_nD_n)$; and
a maximum-likelihood-demodulator for demodulating data output from said discrete filter according to claim 17,
wherein the output waveform of said discrete filter is $(1 - D^2) (c_0 + c_1D + c_2D^2 - c_3D^3)$, and the coefficients (c_0, c_1, c_2, c_3) are $(2, 4, 2, 1)$ respectively.

23. (previously presented) A signal processing circuit comprising:
a discrete filter for converting an input signal into an asymmetrical response;
and

a maximum-likelihood-demodulator for demodulating output from said discrete filter based on said asymmetrical response.

24. (currently amended) A signal processing circuit according to claim 23, wherein said asymmetrical response is selected so as that data modulated demodulated by said maximum-likelihood-demodulator contains a specific error.

25. (previously presented) A signal processing circuit according to claim 23, further comprising:

a register for setting coefficients of said asymmetrical response.

26. (previously presented) A signal processing circuit according to claim 23, wherein the output from said maximum-likelihood-demodulator is directly outputted externally.

27. (previously presented) A signal processing circuit comprising:
an equalizer for equalizing an input signal into a symmetrical response;
a discrete filter for converting the output from said equalizer into an asymmetrical response; and
a maximum-likelihood-demodulator for demodulating output from said discrete filter based on said asymmetrical response.

28. (previously presented) A signal processing circuit according to claim 27, wherein said discrete filter converts so that a data response outputted from said equalizer satisfies a minimum phase transitional condition.

29. (previously presented) A signal processing circuit according to claim 27, further comprising:

an error corrector for correcting at least one bit error among demodulated data output from said maximum-likelihood-demodulator.

30. (previously presented) A signal processing circuit according to claim 27, further comprising:

an error corrector for correcting at least continuous three bits error among demodulated data output from said maximum-likelihood-demodulator.